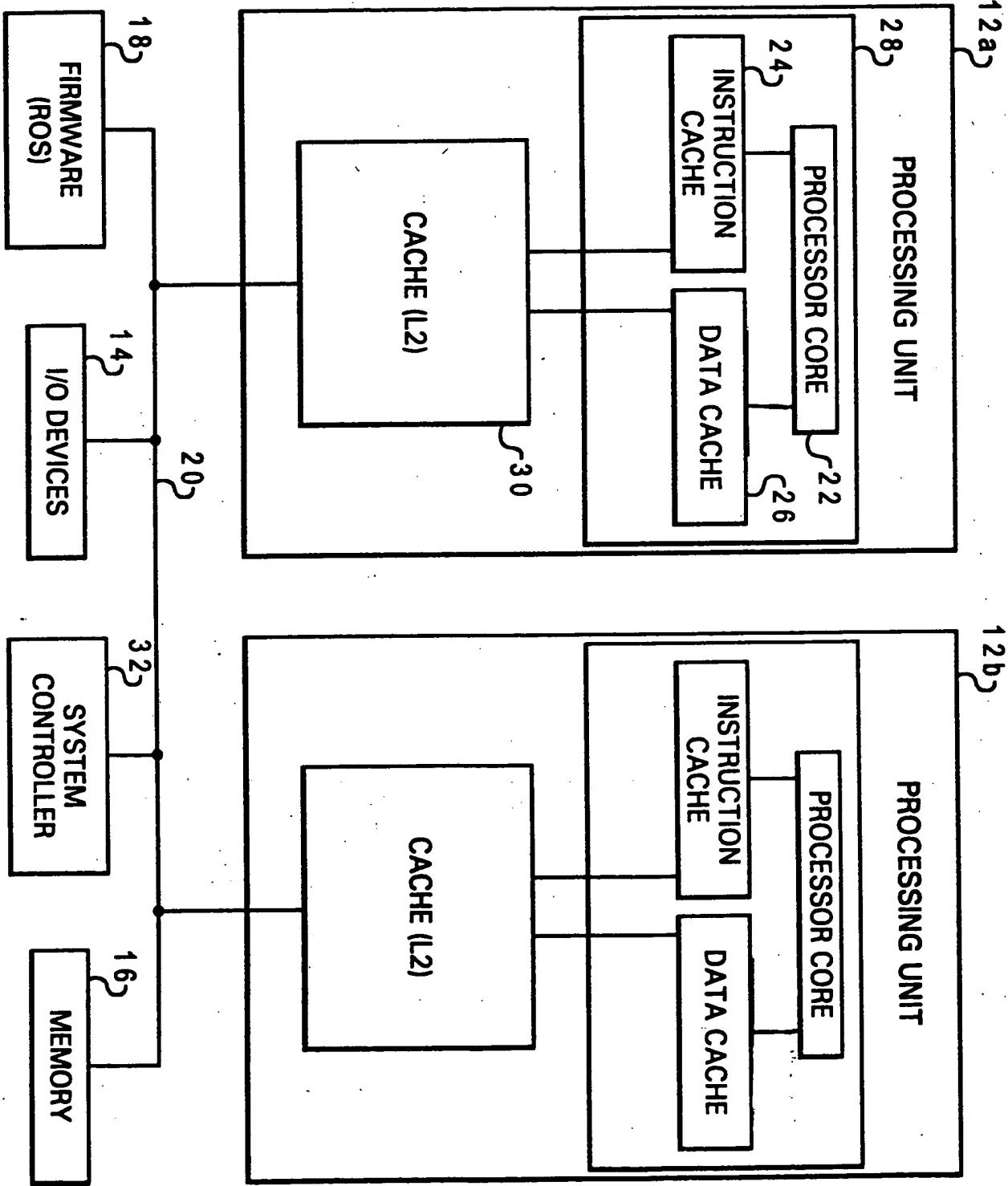


Fig. 1

rt



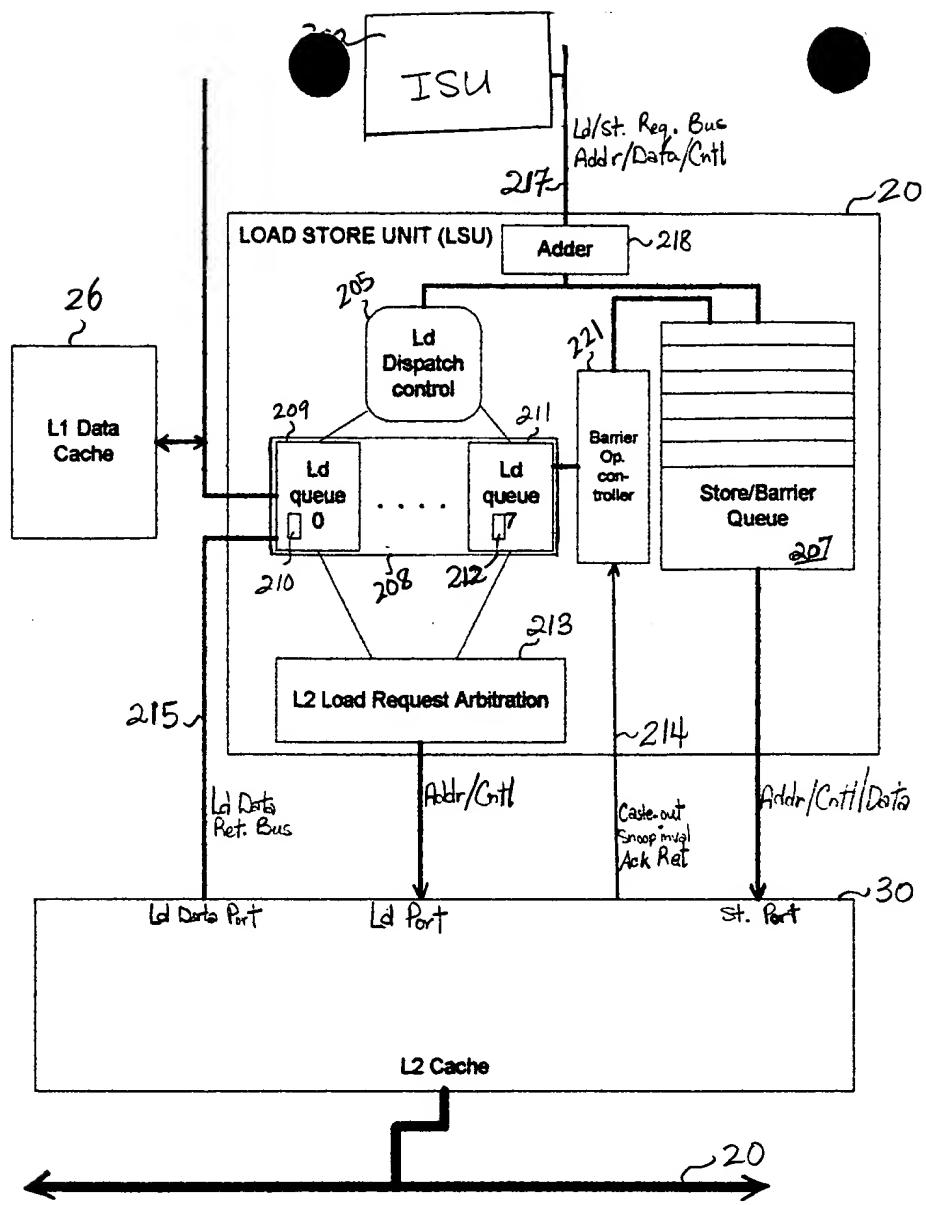


FIG. 2

FIG. 3A

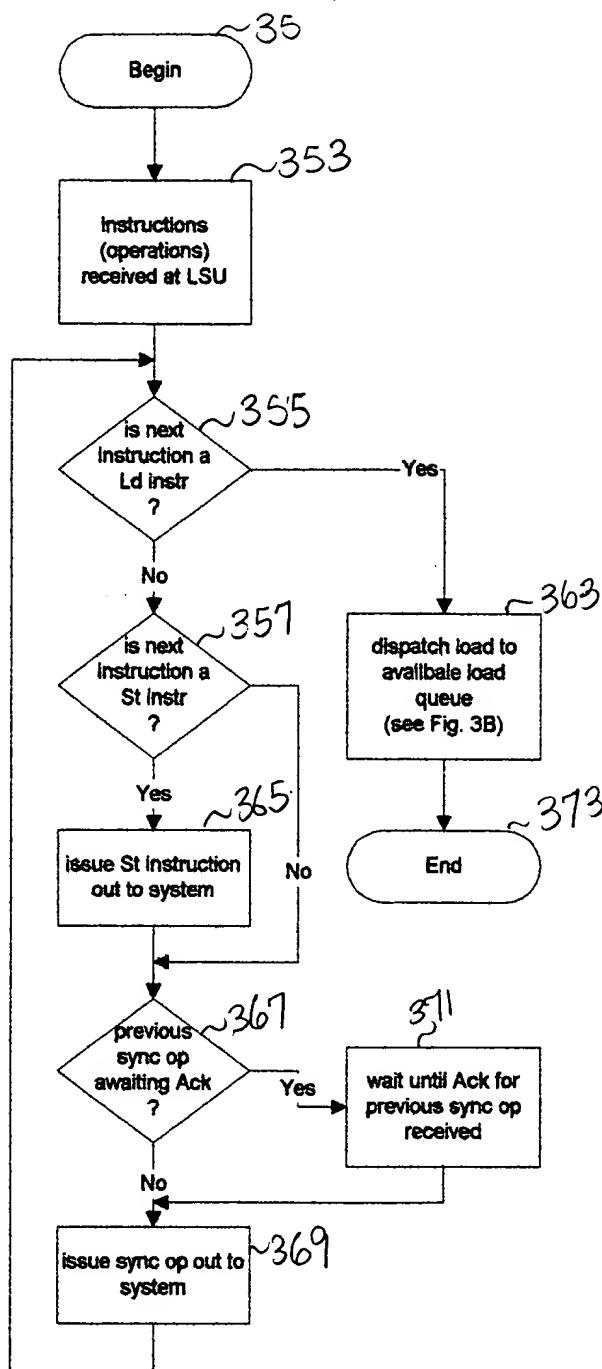


FIG. 3B

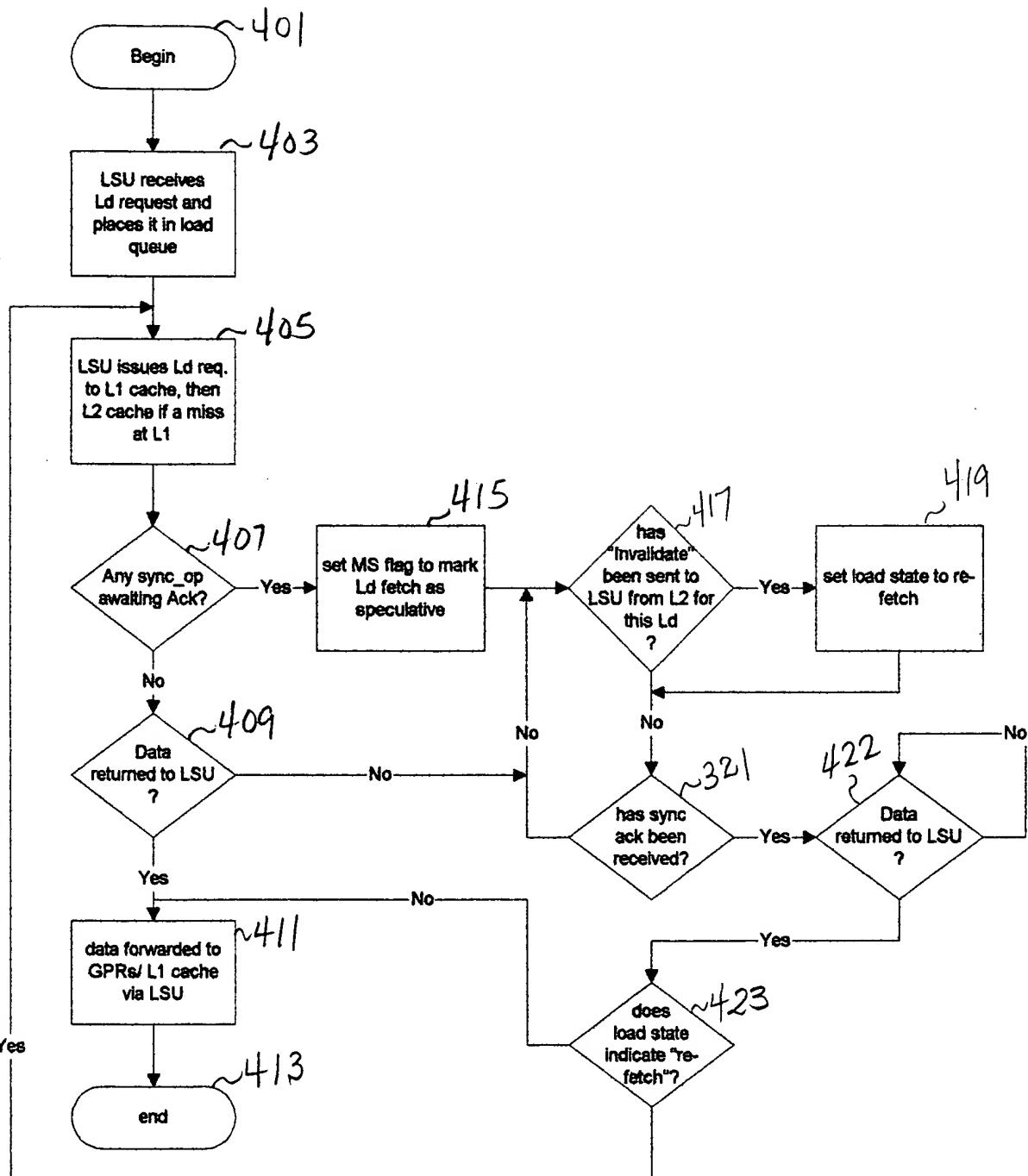


Fig 4A

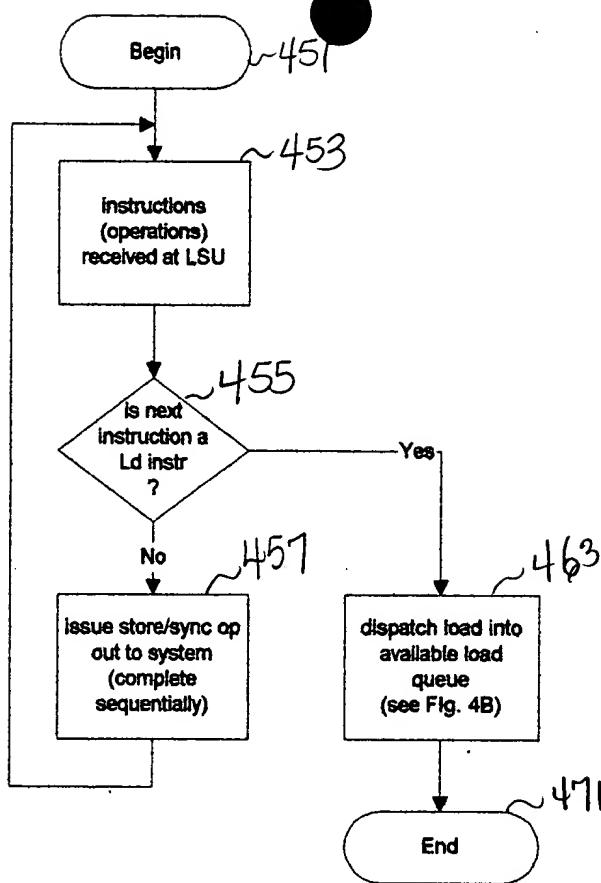


FIG. 4B

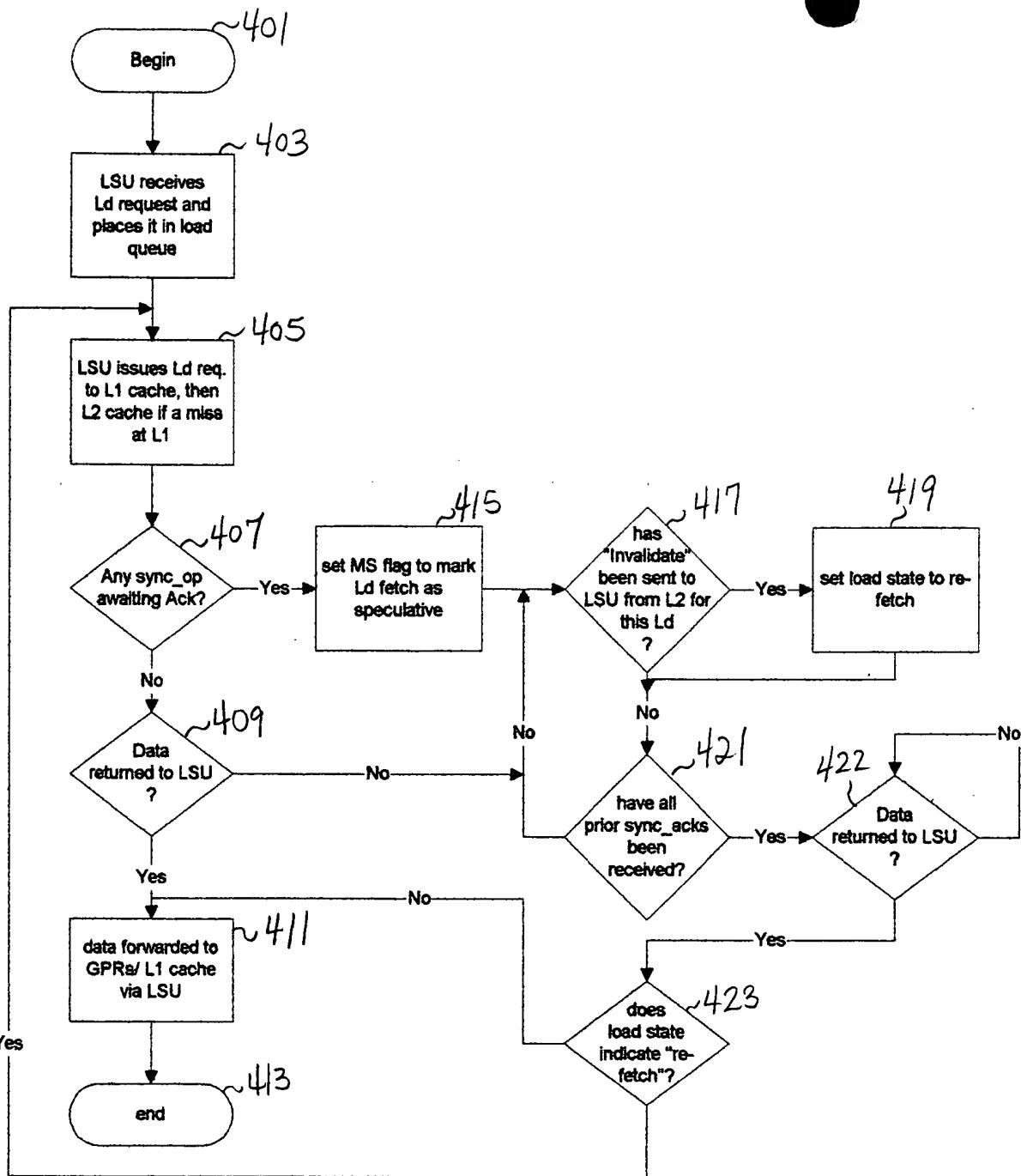


FIG 5

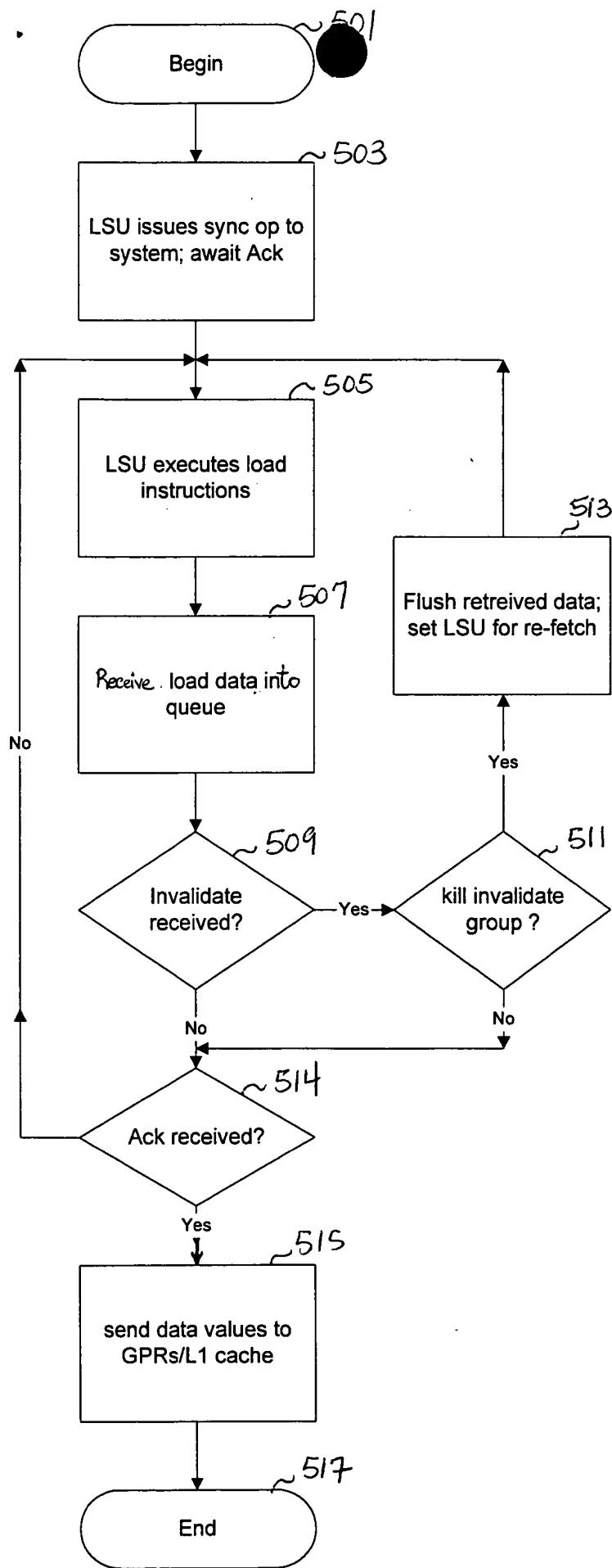


FIG. 8

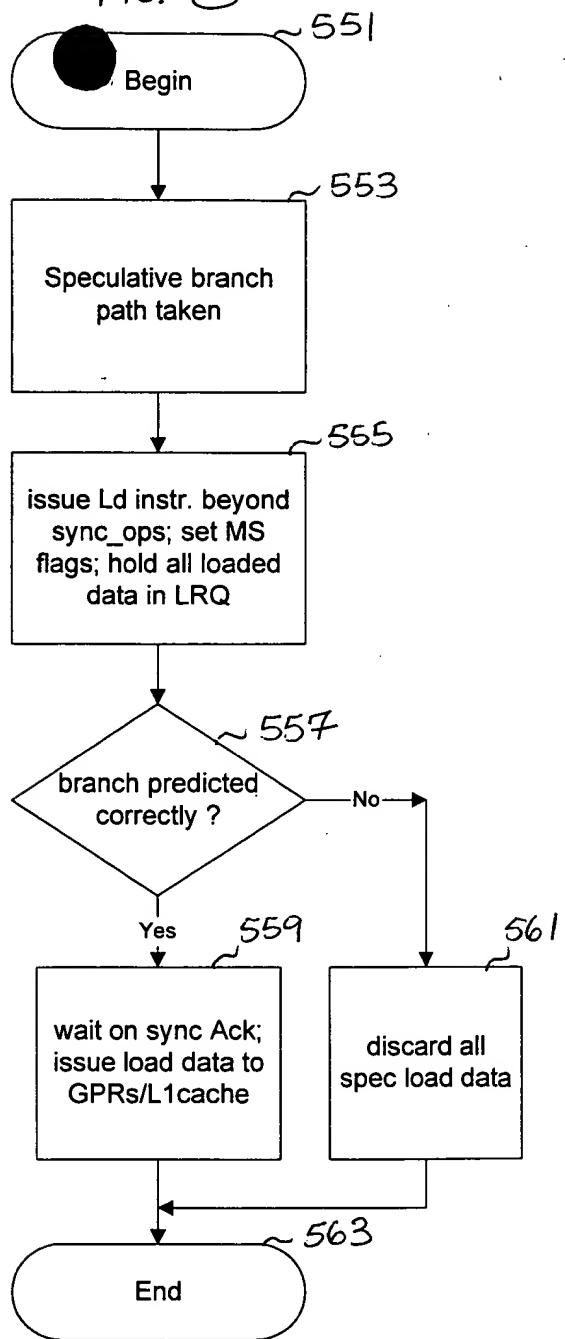


FIG. 6A

- 1) St-An [GROUP A]
- 2) Ld-A0
- 3) Ld-An
- 4) Sync A
- 5) Ld-B0 [GROUP B]
- 6) Ld-Bn
- 7) St-Bn

FIG. 6B

- 1) Ld-A0
- 2) Ld-A1
- 3) St-An
- 4) Sync-A
- 5) Ld-B0
- 6) Ld-B1
- 7) St-Bn
- 8) Sync-B
- 9) Ld-C0
- 10) Ld-C1
- 11) St-Cn
- 12) Sync-C
- 13) Ld-C0
- 14) Ld-C1
- 15) St-Bn
- 16) Sync-D

FIG. 6C

Proc Issue Order	LSU Order to Memory Subsystem	Memory Subsystem Execution order	LSU Completion Order
1) Ld-A0	1) Ld-A0 Sync-A	1) Ld-B0	1) Ld-A0
2) Ld-b0	2) Ld-b0 Sync-B	2) Ld-d0	2) Ld-B0
3) St-C0	3) St-C0 Sync-C	3) Ld-A0	3) St-C0
4) Ld-D0	4) Ld-D0 Sync-D	4) St-C0 5) Sync A, B, C, D	4) Ld-D0

FIG. 6D

Instruction Order	Memory Subsystem Execution Order
St-A0	St-A0
St-A1	St-A1
Sync-A	St-B0
St-B0	St-B1
St-B1	Sync A and B
Sync-B	

FIG. 7

